

## INTERNATIONAL SEARCH REPORT

Int. Patent Application No

PCT/JP03/03036

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 H04L29/12

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H04L G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	GUERRIER P ET AL: "A Generic Architecture for On-Chip Packet-Switched Interconnections" IEEE CONFERENCE PROCEEDINGS, 27 March 2000 (2000-03-27), pages 250-256, XP010377472 USA page 251, left-hand column, line 10 -page 253, right-hand column, line 17 page 254, right-hand column, line 1 - line 54; figures 2-8	1-6
Y	EP 1 083 768 A (ERICSSON TELEFON AB L M) 14 March 2001 (2001-03-14) paragraph '0013! - paragraph '0014! paragraph '0025! - paragraph '0027! paragraph '0036! - paragraph '0043!; claims 13-18; figures 1-6	1-6

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☒ Further documents are listed in the continuation of box C:

☒ Patent family members are listed in annex.

## \* Special categories of cited documents:

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
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- \*P\* document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

17 October 2003

Date of mailing of the international search report

29/10/2003

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>S KUMAR ET AL: "A NETWORK ON CHIP ARCHITECTURE AND DESIGN METHODOLOGY"            IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI, 'Online! April 2002 (2002-04), XP002258216            Pittsburgh, PA, USA            Retrieved from the Internet:            &lt;URL:csdl.computer.org/comp/proceedings/isvlsi/2002/1486/00/14860117abs.htm&gt;            'retrieved on 2003-10-17!            *whole document*</p>	1-6
Y	<p>US 6 381 638 B1 (BORELLA MICHAEL S ET AL)            30 April 2002 (2002-04-30)            column 2, line 47 -column 3, line 42            column 5, line 1 - line 42            column 8, line 45 -column 9, line 23;            claims 1-16; figures 6,7</p>	1-6

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International Application No.  
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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 1083768	A	14-03-2001	EP 1083768 A1	14-03-2001
			AU 6996000 A	10-04-2001
			CA 2383897 A1	15-03-2001
			WO 0119110 A1	15-03-2001
			EP 1210835 A1	05-06-2002
			JP 2003509920 T	11-03-2003
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US 6381638	B1	30-04-2002	NONE	
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